## AMENDMENTS TO THE CLAIMS

Listing Of Claims

Claims 1-28 (Canceled)

29. (currently amended) A method for fabricating a semiconductor component comprising:

providing a semiconductor die comprising a die contact and at least one integrated circuit in electrical communication with the die contact;

forming a polymer layer on the die;

forming a redistribution conductor on the polymer layer in electrical communication with the die contact;

forming a wire bonding pad on the conductor;

forming a first metal layer on the conductor and the wire bonding pad; and

forming a non-oxidizing metal layer on the first metal layer covering the first metal layer and edges thereof configured to seal and protect the conductor and the wire bonding pad and to provide a wire bondable surface.

30. (currently amended) The method of claim 29 wherein the non-oxidizing metal layer comprises a metal selected from the group consisting of Au, Pt ~~or~~ and Pd.

31. (currently amended) The method of claim 29 wherein the first metal layer comprises a metal selected from the group consisting of Ni, V, Cr, CrCu and Cu.

32. (currently amended) The method of claim 29 wherein the forming the first metal layer step and the

forming the non-oxidizing metal layer step comprise electroless deposition.

~~non-oxidizing metal layer covers the bonding pad and the conductor.~~

33. (currently amended) The method of claim 29 further comprising forming a stud bump on the wire bonding pad.

34. (currently amended) The method of claim 29 further comprising wire bonding a wire to the wire bonding pad.

35. (currently amended) The method of claim 29 further comprising forming a second polymer layer on the die and the conductor having an opening aligned with the wire bonding pad.

36. (currently amended) A method for fabricating a semiconductor component comprising:

providing a die comprising a plurality of integrated circuits, a circuit side, and a plurality of die contacts on the circuit side in electrical communication with the integrated circuits having a first pattern;

forming a polymer layer on the circuit side;

forming a plurality of conductors on the polymer layer in electrical communication with the die contacts;

forming a plurality of wire bonding pads on the polymer layer in electrical communication with the conductors and having a second pattern;

forming a plurality of barrier/adhesion layers on the conductors and the wire bonding pads; and

forming a plurality of non-oxidizing layers on the barrier/adhesion layers and edges thereof configured to seal and protect the conductors and the wire bonding pads and to provide wire bondable surfaces.

37. (currently amended) The method of claim 36 wherein the forming the conductors step and the forming the wire bonding pads step comprise electrolessly depositing a first metal.

38. (currently amended) The method of claim 36 wherein the forming the barrier/adhesion layers step comprises electrolessly depositing a second metal.

39. (currently amended) The method of claim 36 wherein the forming the non-oxidizing layers step comprises electrolessly depositing a third metal.

40. (previously presented) The method of claim 36 wherein the polymer layer comprises a material selected from the group consisting of polyimide, PBO and BCB.

41. (currently amended) The method of claim 36 wherein the barrier/adhesion layers comprises ~~a material selected from the group consisting of~~ a metal selected from the group consisting of V, Cr, CrCu and Cu.

42. (currently amended) A method for fabricating a semiconductor component comprising:

providing a substrate comprising a semiconductor die comprising a plurality of integrated circuits and a

plurality of die contacts in electrical communication with the integrated circuits;

forming a plurality of metal bumps on the die contacts;

forming a polymer layer on the die; ~~and~~

planarizing the polymer layer and the metal bumps to a same surface;

forming a plurality of conductors on the polymer layer in electrical communication with the metal bumps, the conductors comprising a plurality of wire bonding pads having a different pattern than the die contacts;

forming ~~a~~ barrier/adhesion layers on the conductors and the wire bonding pads;

forming ~~a~~ non-oxidizing layers on the barrier/adhesion layers and edges thereof configured to seal the conductors and the wire bonding pads and to provide wire bondable surfaces; and

singulating the die from the substrate.

43. (currently amended) The method of claim 42 further comprising forming a plurality of stud bumps on the wire bonding pads.

44. (currently amended) The method of claim 42 further comprising forming a plurality of wire bonds on the wire bonding pads.

45. (currently amended) The method of claim 42 further comprising forming a second polymer layer on the die having openings aligned with the wire bonding pads.

46. (previously presented) The method of claim 42 wherein the substrate comprises a semiconductor wafer.

47. (previously presented) The method of claim 42 wherein the forming the barrier/adhesion layer step comprises electrolessly depositing Ni.

48. (previously presented) The method of claim 42 wherein the forming the non-oxidizing layer step comprises electrolessly depositing Au.

49. (currently amended) A method for fabricating a semiconductor component comprising:

providing a semiconductor die including a circuit side, a plurality of integrated circuits, and a plurality of die contacts on the circuit side in electrical communication with the integrated circuits having a first pattern;

forming a polymer layer on the circuit side;

forming a plurality of conductors on the polymer layer in electrical communication with the die contacts; ~~and~~

forming a plurality of wire bonding pads on the conductors having a second pattern;

forming a plurality of barrier/adhesion layers on the conductors and the wire bonding pads; and

forming a plurality of non-oxidizing layers covering ~~on~~ the barrier/adhesion layers and edges thereof configured to provide wire bondable surfaces.

50. (currently amended) The method of claim 49 further comprising adjusting electrical characteristics of

the conductors by controlling a thickness of the barrier/adhesion layers.

51. (currently amended) The method of claim 49 further comprising forming a second polymer layer on the circuit side encapsulating the conductors and having a plurality of openings aligned with the wire bonding pads.

52. (currently amended) The method of claim 49 wherein the non-oxidizing layers completely seals the conductors and the wire bonding pads.

53. (currently amended) The method of claim 49 further comprising forming a plurality of stud bumps on the wire bonding pads.

54. (previously presented) The method of claim 53 further comprising wire bonding to the stud bumps.

55. (currently amended) The method of claim 49 further comprising wire bonding to the wire bonding pads.

Claims 56-68 (Canceled)